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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,880	07/10/2003	Sabera Kazi	H0004522	8476

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,880	KAZI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/10/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Figure 2, the line pointing at delay element 203 should be corrected so that it does not point to the "best sample section element" element 210.

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: In the "Background of the Invention" section, the description of the conventional DPSK demodulator, paragraph [0011] the quantities Zq(t) Zi(t) shown in Fig. 2 should be identified.

Appropriate correction is required.

Claim Objections

3. Claims 1-21 are objected to because of the following informalities: All of the claims mention the "DPSK" acronym that should be spelled out (at least in the preamble of the independent claims). Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5, 7-9, 11-12, 14-16, 18-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of the current application (hereafter referred to as AAPA) in view of Dutta (U.S. 5,313,493) and Chung et. al. (U.S. 2004/0190655).

With respect to claim 1, the AAPA discloses:; a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components with a first delayed, conjugated version of the in-phase and quadrature components (see Fig. 2, section "differential demodulator" including elements 203, 204, 204 and signals processed there are understood to be complex (in-phase and quadrature) since the conjugate operation of element 204 is meaningful for complex signals, see paragraph [0007] of the specification) ; a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an

oscillator in the DPSK transmitter (Fig. 2, element 218, see paragraph [0011] of specification); a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase (Fig. 2, phase out of element 220, see last sentence of paragraph [0011] of the specification); a phase correction circuit to determine an absolute phase using the corrected phase (Fig. 2, elements 224, 226, see paragraph [0012]); and a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data (Fig. 2, element 226, see last sentence of paragraph [0012]).

The AAPA does not expressly teach: means for converting the input signal to in-phase and quadrature components, and a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components.

In the same field of endeavor, Dutta discloses: means for converting the input signal to in-phase and quadrature components (see column 1, lines 46-51). At the time of the invention, it would have been obvious to a person skilled in the art to use complex baseband signal representation i.e. convert the input signal to in-phase and quadrature components in the receiver of the AAPA that includes the DPSK demodulator of Fig. 2, since DPSK information is contained in a vector including I and Q components (see Fig. 1 of the instant application).

In the same field of endeavor, Chung et. al., a frequency offset calculation circuit to determine a frequency offset by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components (see Fig. 1, output $\Delta\theta$ is the phase increment caused by frequency offsets (mentioned in middle of paragraph [0005] that describes the apparatus shown in Fig. 1) .

At the time of the invention, it would have been obvious to a person skilled in the art to use the frequency offset determining system of Chung et. al., in the system of the AAPA (substituting elements 218 and 220 since the system of Chung et. al, determines the phase offset caused by the frequency offset, therefore, element 220 is unnecessary) since (carrier) frequency offsets must be determined and corrected since they introduce phase rotation to the ideal signal phasor (i.e. distort the signal) (see paragraphs [0002]-[0004] of Chung et. al., where the (carrier) frequency offset is undesirable to the signal and has to be corrected).

With respect to claim 2, all of the limitations of claim 2 are analyzed above in claim 1, except for: comprising a glitch filter to filter the frequency offsets to remove noise and glitches caused by phase transients between symbols.

However, Chung et. al., discloses: removing noise and glitches caused by phase transients between symbols, see squaring operation of element 20 of Fig. 1, and second half of paragraph [0005] and all of paragraphs [0006]-[0007], where the squared phasor (that includes the frequency offset) that is insensitive to phase differences between successive modulated samples (understood to also include phase errors

(transients) caused for example by non-ideal components), and see that the noise can be ignored). Therefore at the time of the invention, it would have been obvious to a person skilled in the art that the system (squaring, averaging operation) of Chung et. al., functions equivalently to a glitch filter that removes noise and glitches caused by phase transients between symbols.

With respect to claim 3, all of the limitations of claim 2 are analyzed above in claim 1, and the AAPA disclose: wherein the delay associated with the first delayed version of the I and Q components in the differential demodulator is approximately one symbol interval (see Fig. 2, delay Z has Tsym duration and see last sentence of paragraph [0007] of specification).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit to determine an optimal sample to use to determine the demodulated phase and the frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0009] of the specification).

With respect to claim 7, all of the limitations of claim 7 are analyzed above in claim 5, and claim 7 is analyzed similarly to claim 2 above.

With respect to claim 8, claim 8 is analyzed similarly to claim 1 above, and with respect to the limitations: receiving the DPSK signal; digitizing the DPSK signal, in the same field of endeavor, Dutta et. al., discloses: receiving the PDPSK signal; digitizing the PDPSK signal (see Fig. 4, the PDPSK communication system, receiver and transmitter, the receiver includes antenna to received the transmitted PDPSK signals and see column 7, lines 35-38 where digital signal implies converting to digital signals at the receiver side of Fig. 4). At the time of the invention, it would have been obvious to a person skilled in the art that receiving the DPSK signal (with an antenna as shown by Dutta for the PDPSK signal) and digitizing the DPSK signal (as implied by Dutta) since receiving and digitizing signals is very well in the art and is an integral part of communication receivers and allows for use of DSPs (allow for fast processing, miniaturization since they can be combined with other digital components).

With respect to claims 9, 11, 12, 14 these claims are analyzed similarly to claims 3, 2, 5, and 7 above.

Claims 15, 16, 18-19, 21 are analyzed similarly to claims 1, 3, 2, 5, and 7 above.

6. Claims 1, 3-5, 8- 10,12 15, 17 are rejected under 35 U.S.C. 103(a) being unpatentable over the applicant's admitted prior art of the current application (hereafter referred to as AAPA) in view of LaBerge et. al. (U.S. 5,142,287).

With respect to claim 1, the AAPA discloses:; a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components with a first delayed, conjugated version of the in-phase and quadrature components (see Fig. 2, section "differential demodulator" including elements 203, 204, 204 and signals processed there are understood to be complex (in-phase and quadrature) since the conjugate operation of element 204 is meaningful for complex signals, see paragraph [0007] of the specification) ; a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter (Fig. 2, element 218, see paragraph [0011] of specification); a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase (Fig. 2, phase out of element 220, see last sentence of paragraph [0011] of the specification); a phase correction circuit to determine an absolute phase using the corrected phase (Fig. 2, elements 224, 226, see paragraph [0012]); and a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data (Fig. 2, element 226, see last sentence of paragraph [0012]).

The AAPA does not expressly teach: means for converting the input signal to in-phase and quadrature components, and a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components.

In the same field of endeavor, LaBerge et. al. disclose: means for converting the input signal to in-phase and quadrature components (see column 2, lines 54-56), and a frequency offset calculation circuit to determine a frequency offset between the DPSK receiver and the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components (see abstract, column 5, lines 43-44, and column 4, lines 56-64, interpreted as referring to phase rotation cause caused by unknown frequency drift, (see for example Doppler shifts mentioned in column 4, lines 60-66) and also see column 6, lines 42-45, where phase wT or wT + π cane be determined).

At the time of the invention, it would have been obvious to a person skilled in the art to use the apparatus and teachings of LaBerge et. al., (for example as shown in Fig. 7, the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector) that process complex signals, and generate Vc(t), see column 6, lines 42-45 out of which the phase offset corresponding to the frequency error), to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components, (similarly to the Doppler shift caused frequency error, non-ideal components such as oscillators also contribute to frequency errors) since it is known in the art that frequency errors/shifts result into phase shifts that distort the received signals and have to be taken into account and compensated for at the receiver (also see abstract of LeBerge et. al.).

With respect to claim 3, all of the limitations of claim 2 are analyzed above in claim 1, and the AAPA disclose: wherein the delay associated with the first delayed version of the I and Q components in the differential demodulator is approximately one symbol interval (see Fig. 2, delay Z has Tsym duration and see last sentence of paragraph [0007] of specification).

With respect to claim 4, all of the limitations of claim 4 are analyzed above in claim 1, and LaBerge et. al., discloses: wherein the delay associated with the I and Q components in the frequency offset calculation circuit is approximately one sample interval (see abstract, (especially the ...removal of effects of unknown frequency component...) and column 4, lines 7-13, 45-60, where the sample interval is interpreted to correspond to the bit time and also see column 5, lines 66-67, and column 6, lines 1-18, 42-45, where the phase corresponding to the wT is the unknown frequency rotation (column 5, lines 43-44)).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit to determine an optimal sample to use to determine the demodulated phase and the frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0009] of the specification).

With respect to claim 8, claim 8 is analyzed similarly to claim 1, above and with respect to the additional limitations: receiving the DPSK signal; digitizing the DPSK signal;, LaBerge et. al., disclose the above in column 3, lines 43-45, 52-67, (reception of IF signal that uses DPSK, and A/D conversion of the received signal)

With respect to claims 9-10, 12, these claims are analyzed similarly to claims 3-5 above.

With respect to claims 15, 17 these claims are analyzed similarly to claims 1,3-5 respectively.

7. Claims 6, 13, 20 are rejected under 35 U.S.C. 103(a) being unpatentable over the applicant's admitted prior art of the current application (hereafter referred to as AAPA) in view of LaBerge et. al. (U.S. 5,142,287) as applied to claims 5, 12, 19 respectively, and in view of Legrand et. al., (U.S. 6,74,822).

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 5, except for: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude of the combined in-phase and quadrature components of each sample in each symbol interval.

In the same field of endeavor, Legrand et. al., disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude each sample in each symbol interval (see column 1, lines 62-67, column 2, lines 7, column 3, lines 40-42, where the sample (and subsequently the

sampling instant) with the maximum value is determined and keeps updating). At the time of the invention, it would have been obvious to a person skilled in the art at the time of the invention, to use the teachings of Legrand in the system of the AAPA, to determine the optimal sample as the sample associated with a peak amplitude (maximum value) of the combined in-phase and quadrature components of each sample in each symbol interval (the combined in-phase and quadrature components would be used since the system of AAPA processes complex signals and finding the peak value of the samples would involve using the in-phase and quadrature components). The benefit of using the teachings of Legrand et. al., in the system of the AAPA (to perform best sample selection) include: limiting the number of computations and operating costs (see column 1, lines 49-51 of Legrand et. al.,)

With respect to claims 13, and 20 these claims are analyzed similarly to claim 6 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hunag et. al., (U.S. 5,991,289) disclose: a method and system for symbol, frame , and carrier synchronization for OFDM signals.

Mui (U.S. 5,432,819) discloses: a phase and frequency trackers used in a DPSK receiver.

Dutta (U.S. 5,450,447) discloses: AFC loop used in a PSK based system.

Kim (U.S. 7,058,151) discloses: frequency and timing synchronization for OFDM signals.

Tsuda et. al., (U.S. 5,440,267): a pi/4 shift QPSK receiver using a frequency error offset estimating circuit that corrects for transmitter/receiver frequency offsets.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
10/12/2006

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